Power Efficient Comparators for Long Arguments in Superscalar Processors

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Outline

- Motivations
- 8-bit comparator designs
  - Traditional Comparator
  - Dissipate on Match Comparator (ICCD’02)
- 32-bit Comparator Designs
- Results: Application to the Load-Store Queue
- Conclusions
Motivation

Equality comparators are very pervasive in today’s superscalar datapaths.
- Wake-up logic of the Issue Queues
- Dependency checking logic
- Load-Store queues
- Translation Lookaside Buffers (TLB)
- Caches
- Branch Target Buffers (BTB)
Motivation (continued)

- Traditional comparators dissipate energy on mismatches in any bit position of the arguments.
- In many cases, mismatches are much more frequent than matches.
  - Issue queue: Only 3% of all comparisons result in a match (Ergin et al., ICCD’02)
- For energy efficiency, dissipate-on-match designs can be considered.
Traditional 8-bit Pull-Down Comparator
Dissipate-on-Match Comparator (DMC, ICCD’02)
Use of the Long Comparators

- Load-Store queues – to allow loads to bypass earlier stores
- TLBs – for associative lookup
- Caches – for associative lookup
- BTBs – for associative lookup
Traditional 8-bit Pull-Down Comparator
Dissipate-on-Match Comparator (DMC)
Comparison of larger operands: Some Alternatives

(a) 32-bit traditional comparator

(b) 32-bit dissipate-on-match comparator

(c) 32-bit energy-efficient comparator: variation 1

(d) 32-bit energy-efficient comparator: variation 2

(e) 32-bit energy-efficient comparator: variation 3

Each TRAD compares 8 bits
Each DMC compares 8 bits
Each DMC and TRAD compares 8 bits
Each DMC compares 8 bits

~270 ps
~270 ps
~270 ps
>400 ps
>400 ps
Choosing the Right Alternative

Need to consider impact on:
- Delay
- Energy

Have to look at distributions of bit values that are compared

More than one alternative may be acceptable
Experimental Setup (AccuPower, DATE’02)

- Compiled SPEC benchmarks
- Datapath specs
- Microarchitectural Simulator
  - Performance stats
    - Transition counts, Context information
- VLSI layout data
- SPICE deck
- SPICE
  - Energy/Power Estimator
    - Power/energy stats
    - SPICE measures of Energy per transition
Matching Statistics of 32-bit Addresses in the LSQ

Number of matching bit pairs in each of the 4 8-bit groups
Dissipate-on-Match Comparator (DMC)
Matching Statistics of 32-bit Addresses in the LSQ

Number of matching bit pairs in each of the 4 8-bit groups
Energy savings in comparison of longer operands

(a) 32-bit traditional comparator

(b) 32-bit dissipate-on-match comparator

(c) 32-bit energy-efficient comparator: variation 1

19% Energy Increase  19% Energy Savings
Main Results

- We discussed some energy-efficient 32-bit wide comparator designs.
- 19% comparator-related energy reduction in LSQ is achieved by using a hybrid design (3 TRADs + 1 DMC) compared to the use of 4 TRAD comparators.
- Results can be extended to TLBs and BTBs.
THANK YOU!

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Timing Diagrams

Proposed comparators

Traditional comparator

$t_{pre}$

$t_{prop}$

$t_{dis}$

$t_{eval}^*$

$t_{eval}$

$t_{pre}$

$t_{cycle}$
32-bit Matching Statistics: LSQ
Traditional 8-bit Pull-Down Comparator
## Pass Logic, Single-Stage Comparator (PLSSC)

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<th>Energy of the 8-bit DMC used to build a 32-bit comparator (fJ)</th>
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