

PhD Exam – Spring 2004 – Design Automation
Answer as much of the seven questions as you can.

1. Outline the basic design flow for an IC, from start to manufacture.
2. System delay has shifted in the past few year; what was the “slow link” in a system 10 years ago? What’s slow now? Why?
3. “Multi-level” optimization has been gaining attention in design automation; describe at a high level the approach (you might want to include a “v-cycle” picture).
4. Outline the basic algorithm for simulated annealing; describe the parameters that affect run time.
5. Sketch pseudocode for the 1-Steiner heuristic.
6. Sketch pseudocode for the Borah-Owen-Irwin Steiner heuristic.
7. Describe the bucket data structure used by the Fiduccia-Mattheyses partitioning heuristic.
8. Most routing tools use a “rip-up and reroute” approach; describe how this works.
9. Subwavelength lithography has made physical design more complex; describe some new constraints that are caused by lithography requirements, and some of the common “fixes.”
10. Describe a problem in design automation that is worthy of the attention of a PhD student for the next few years (ok, you can change—just seeing what ideas you have).