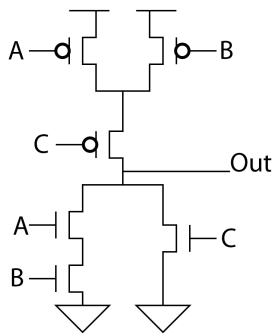


Name:

CS210 Fall 2007 Exam 2

Every question is worth 5 points unless noted otherwise.

1. Draw P and N transistors (and label them).
2. Draw an Inverter at the transistor level.
3. Draw a two-input NAND gate at the transistor level.
4. Create a truth table for this circuit.



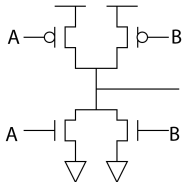
5. Draw a two-bit decoder.

6. Draw a two-input MUX (using AND and OR gates).

7. Draw an R-S Latch.

8. (2 points) A gated D latch contains an R-S latch; it has inputs normally labeled “D” and “WE”. What does “WE” stand for (or what does it do)?

9. (3 points) This circuit may short out (connect power to ground). What input patterns would do that?



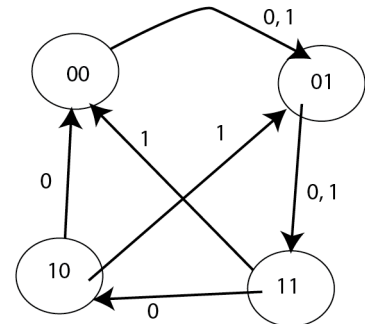
10. Suppose we have a memory, with address lines A[0,1], a WE input, and data lines D[0,1,2]. The inputs to the memory (in the following order) for a series of clock cycles are:

A0	A1	WE	D0	D1	D2
0	1	1	1	0	1
1	0	0	0	0	1
1	1	1	1	1	0
0	0	1	0	0	0
1	1	0	1	0	0
1	0	0	1	1	1

The memory has four 3-bit words. Show what's in each of them. If you can't determine what's in a memory location, put a question mark.

1. For this sequential finite state machine, you can have a truth table that lists the “next state.” Fill in the truth table. NS0 and NS1 the next state.

S0	S1	Switch	NS0	NS1



2. Suppose we have 5 bits to hold the state of a finite state machine. How many different states will we be able to have?
3. Suppose we have a state machine with 9 states. How many bits will we need to have to run the machine?
4. Suppose we want to build a circuit to implement the Boolean function $(A \oplus B C) + (A B C)$. Draw the Karnaugh map for this circuit, circle the rectangles, and show what the simplified version of the circuit would be (either a Boolean function, or a circuit with AND and OR gates).
5. Draw the Karnaugh map for inputs S0, S1, Switch, and output NS0, from question 11.

