

Call for Papers

1st Workshop on Architectural Reliability (WAR-1)

November 13, 2005 - Barcelona, Spain

<http://www.cs.binghamton.edu/~oguz/war2005>

to be held in conjunction with

the 38th International Symposium on Microarchitecture (MICRO-38)

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Submission

Authors are requested to submit their work in IEEE format, not exceeding 10 pages. Submitted files must be viewable by using Acrobat Reader. Manuscripts must be sent to osmanx.unsal@intel.com via e-mail not later than 22 September 2005 along with the author affiliations and contact information.

Important Dates

Paper submission: September 22

Author notification: October 8

Final version due: October 22

Workshop Theme:

Following performance and power, reliability has emerged as the latest challenge in microarchitecture. Various developments have combined to make reliability a concern: soft-error rate is projected to increase with scaling; variability due to non-deterministic placement of dopant atoms and channel length is increasing design margins; better than worst-case design techniques for power/performance require error detection/correction; aggressive application of power-saving mechanisms such as clock- and V_{dd}-gating are increasing voltage droops; the verification manpower budget is becoming a significant part of the design effort; oxide breakdown and electromigration are decreasing processor lifetimes...

WAR will serve as a forum for microarchitectural solutions to address such current and emerging reliability-related issues. Although the focus is on architecture, work on synergistic circuit, compiler, OS and network solutions is also encouraged. Through sharing ideas and fermenting further research, the inaugural workshop will hopefully serve to make WAR an annual event in this exciting new area.

Topics of Interest:

- Soft-error measurement, modeling and mitigation techniques
- Lifetime reliability
- Better than worst case design
- Dynamic verification techniques
- Approximate processing and reliability
- Techniques for reducing impact of:
 - Temperature
 - Voltage droops, di/dt swings
 - Process variation
 - Crosstalk
- Fault tolerance
 - Fault injection
 - Fault detection
 - Error modeling
 - Fail-safe and fail-stop systems
 - Time and space redundancy
 - dRedundancy/dEnergy (dR/dE) -efficient architectures
- Compiler/architecture/OS techniques and interaction for reliability