Meltem Ozsoy

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Experience

Intel **May 2012 – Dec 2012**

Graduate Technical Intern (Avoton Project)
Performance studies for multicore microservers, worked on Intel Avoton processor simulator

Binghamton University **Aug 2009 - Present**

Teaching Assistant – (Jan 2013 – Present)
Computer Organization and Architecture

Research Assistant – (Aug 2009 – May 2012)
Architectural Support for Trusted Computing in Many-core Processors

TOBB University of Economics and Technology **Sep 2008 – Jul 2009**

Research Assistant (TUBITAK)
Reducing the Power Dissipation of Out-of-Order Microprocessors by Detecting Narrow Values and Narrow Value Phases

Vivante **May 2008 – Aug 2008**

Intern (GC-100 Project)
Rasterizer algorithm implementation with Visual C#

Education

Ph.D. Computer Science. Binghamton University. **Aug 2009 – Aug 2014 *(expected graduation)***

Co-advisors: Dmitry Ponomarev, Nael Abu-Ghazaleh

M.S. Computer Engineering. TOBB University of Economics and Technology. **Sep 2008 – Jul 2009**

Advisor: Oguz Ergin

B.S. Computer Engineering. TOBB University of Economics and Technology. **Sep 2004 – Aug 2008**

Publications

- **Dynamic Associative Caches: Reducing Dynamic Energy of First Level Caches** *(submitted)*
  Karthikeyan Dayalan, Meltem Ozsoy and Dmitry Ponomarev; *International Symposium on Low Power Electronics and Design (ISLPED'14),* Aug 2014
- **ASENA: An Architectural Sub-semantic Engine for Malware Detection** *(submitted)*
  Meltem Ozsoy, Iakov Goreli, Nael Abu-Ghazaleh and Dmitry Ponomarev; *23rd Usenix Security Symposium*, Aug 2014
- **Efficient Dynamic Information Flow Tracking on SMT Processors**
  Meltem Ozsoy, Dmitry Ponomarev, Nael Abu-Ghazaleh and Tameesh Suri; *IEEE Transactions on Computers*, vol.63, no.2, pp.484,496, Feb. 2014
- **Efficiently Securing Systems from Code Reuse Attacks**
  Mehmet Kayaalp, Meltem Ozsoy, Nael Abu-Ghazaleh and Dmitry Ponomarev*; IEEE Transactions on Computers*, Nov 2012
- **Branch Regulation: Low-Overhead Protection from Code Reuse Attacks**
  Mehmet Kayaalp, Meltem Ozsoy, Nael Abu-Ghazaleh and Dmitry Ponomarev*; 39th International Symposium on Computer Architecture (ISCA'12)*, June 2012

- **SIFT: A Low-Overhead Dynamic Information Flow Tracking Architecture for SMT Processors**
  Meltem Ozsoy, Dmitry Ponomarev, Nael Abu-Ghazaleh and Tameesh Suri*; 8th ACM International Conference on Computing Frontiers (CF '11)*, May 2011
- **Dynamic Register File Partitioning in Superscalar Microprocessors for Energy Efficiency**
  Meltem Ozsoy, Yusuf Onur Kocberber, Mehmet Kayaalp and Oguz Ergin; *28th International Conference on Computer Design (ICCD'10)*, October 2010
- **Wireless Computer Architecture**
  Oguz Ergin, Yusuf Onur Kocberber, Meltem Ozsoy; *First Embedded Systems and Applications Symposium, GömSis 2008*, Istanbul, November 2008

Skills

- Programming Languages: C, C++, C#, Java, Verilog HDL, FPGA Programming Tools, Assembly
- Design/Power Tools: Microarchitecture Simulators (PTLsim, MSim, SimpleScalar), Wattch, PIN, CACTI
- Scripting Languages: Perl, PHP, GAWK
- Visual languages: Visual Basic, VC++, Visual C#
- Others: Octave, Matlab, GNUPlot, Machine Learning

Projects

- *Reducing Dynamic Energy of Caches*
  Reorganization of set associative caches for energy efficiency without sacrificing the processor performance.
- *ASENA: An Architectural Sub-Semantic Engine for Malware Detection*
  Studied architectural features for malware detection, accomplished online detection with 85% classification accuracy with 10% false positive rate and implemented the detection unit on hardware using Verilog HDL.
- *Architectural Support for Trusted Computing in Many-Core Processors*
  Investigating energy efficient and high performance techniques for dynamic information flow tracking using spare cores and thread contexts of a multicore processor (CF'11 and IEEE TC). Extending these ideas to other forms of program monitoring.
- *Reducing the Power Dissipation of Out-of-Order Microprocessors by Detecting Narrow Values and Narrow Value Phases*
  A dynamic mechanism based on data width for energy efficiency on register files; details are presented in the paper in proceedings of the 28th ICCD.
- *Kasırga - Processor Design Project (CPUTurkey 2008 Competition 2nd Rank Visual Design Category)*
  16 bit, 4 stage pipelined processor with static branch prediction, 95 Mhz frequency on Xilinx Spartan 3e FPGA, designed with Verilog HDL
- *GC-100 (GPU Design Project)*
  Graphical Processor Unit designed on Altera Nios II FPGA Kit

Academic Activities and Presentations

- *[Attendee] Trusted Infrastructure Workshop 2010*
  Pittsburgh, PA, June 7-11, 2010
- *[Attendee] CRA-W/CDC Workshop on Diversity in Design Automation and Test*
  Pittsburgh, PA, May 23-24, 2011
- *[Attendee] SCA: Tutorial on Introduction to Security for Computer Architects (In conjunction with ISCA'11)*
  San Jose, CA, June 4-8, 2011
- *[Presenter] Using Content-Aware Bitcells to Reduce Static Energy Dissipation*
  F.Koc, O. Simsek and O. Ergin; ICCD'11, Amherst, MA, October 9-12, 2011
- *[Presenter] Architectural Support for Software Security; CRA-W Graduate Cohort Workshop*
  Boston, MA, April 5-6, 2013
- *[Presenter] Dynamic Information Flow Tracking on SMT Processors*
  Binghamton University Computer Science Graduate Students Organization Meeting, 2013
- *[Presenter] Intel Performance Monitoring Unit*
  Binghamton University Computer Science Graduate Students Organization Meeting, 2014