Jason Loew

Curriculum Vitae

Contact

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Employment

9/2010–present
Research Assistant
Department of Computer Science, State University of New York at Binghamton (SUNY Binghamton), Binghamton, NY

5/2007–5/2010
Instructor of Record
Department of Computer Science, SUNY Binghamton
Undergraduate Computer Architecutre - Spring 2010
Undergraduate Data Structures - Summer 2007, Summer 2008
Graduate Programming Fundamentals - Fall 2007

1/2009–12/2009
Co-Instructor
Department of Computer Science, SUNY Binghamton
Undergraduate Computer Architecture - Spring 2009, Fall 2009

8/2005–5/2009
Teaching Assistant
Department of Computer Science, SUNY Binghamton
Graduate Computer Architecture - Spring 2008
Undergraduate Introduction to Programming - Fall 2006, Fall 2007
Undergraduate Data Structures - Fall 2005, Spring 2007
Undergradute Computer Systems - Spring 2006

8/2003–5/2004
Teaching Assistant
Department of Psychology, SUNY Binghamton
Undergraduate Lab in General Psychology - Fall 2003, Spring 2004
Undergraduate Multicultural Psychology - Spring 2002

Education

- *Ph.D., Computer Science*, Expected May 2011, SUNY Binghamton
  Thesis: *Managing Resources of Multicore and Multithreaded Processors for Performance and Security*
- *M.S., Computer Science*, August 2006, SUNY Binghamton
  Thesis: *Quantifying the Impacts of Disabling Speculation and Relaxing the Scheduling Loop in Multithreaded Processors*
- *B.S., Computer Science*, May 2004, SUNY Binghamton,
- *B.A., Psychology*, May 2004, SUNY Binghamton
- *Certificate in College Teaching*, Expected May 2011, SUNY Binghamton
- *Certificate in Community College Teaching*, Expected May 2011, SUNY Binghamton

Honors and Awards

Graduate Student Award for Excellence in Teaching
Awarded for 2007-2008

Clifford D. Clark Graduate Fellowshop
Awarded for 2004-2009

Stipend supported by NSF-AGEP grant to improve teaching skills
Awarded for Spring 2009, Fall 2009 and Spring 2010

Memberships

2009–2010	Member, Institute of Electrical and Electronics Engineers (IEEE)
2007–present	Member, Association of Computing Machinery (ACM)

Publications

Conference and Journal Papers

Jared Schmitz, **Jason Loew**, Jesse Elwell, Dmitry Ponomarev, and Nael Abu-Ghazaleh. TPM-SIM: A Framework for Performance Evaluation of Trusted Platform Modules. In *The 48th Design Automation Conference (DAC)*, June 2011.

Jason Loew, Jesse Elwell, Patrick Madden, and Dmitry Ponomarev. A Co-Processor Approach for Accelerating Data-Structure Intensive Algorithms. In *28th IEEE International Conference on Computer Design (ICCD 2010)*, pages 431–438, October 2010.

Jason Loew, Patrick Madden, and Dmitry Ponomarev. Customized Architectures for Faster Route Finding in GPS-Based Navigation Systems. In *8th IEEE Symposium on Application Specific Processors (SASP 2010)*, pages 36–43, June 2010.

Jason Loew and Dmitry Ponomarev. A Two-Tiered Modeling Framework for Undergraduate Computer Architecture Courses. In *Workshop on Computer Architecture Education (WCAE 2009) held in Conjuction with the 42nd International Symposium on Microarchitecture (MICRO 2009)*, pages 24–29, December 2009.

Jason Loew and Dmitry Ponomarev. Aggressive Scheduling and Speculation in Multithreaded Architectures: Is It Worth Its Salt? In *20th International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)*, pages 11–18, October 2008.

Joseph Sharkey, **Jason Loew**, and Dmitry Ponomarev. Reducing Register Pressure in SMT Processors through L2-Miss-Driven Early Register Release. *ACM Transactions on Architecture and Code Optimization (ACM TACO)*, 5(3), November 2008.

Jason Loew and Dmitry Ponomarev. Two-Level Reorder Buffers: Accelerating Memory-bound Applications on SMT Architectures. In *37th International Conference on Parallel Processing (ICPP)*, pages 182–189, September 2008.

Invited Papers

Jason Loew, Jesse Elwell, Dmitry Ponomarev, and Patrick Madden. Mathematical Limits of Parallel Computation for Embedded Systems. In *16th Asia and South Pacific Design Automation Conference (ASP-DAC 2011)*, pages 653–660, January 2011.

Research Summary

The microprocessor design industry has recently undergone a fundamental shift from complex single-core architectures to designs that rely on the use of multiple cores and multiple thread contexts.

My research first examined the microarchitecture of a single simultaneously multithreaded (SMT) microprocessor. In this design, multiple thread contexts execute simultaneously while sharing most of the existing datapath resources. We proposed a low complexity mechanism for accelerating memory-bound threads on SMT processors without adversely impacting the performance of other concurrently running applications. The main idea is to provide a two-level organization of the Reorder Buffer (ROB), where the first level is comprised of small private per-thread ROBs which are used in the normal course of execution in the absence of last level cache misses. The second ROB level is a much larger storage that can be used on demand by threads experiencing last level cache misses.

Second, we examined the design of future multi-core and many-core systems. One of the promising directions in this vein of research is to utilize the spare cores of a multicore processor for various co-processing tasks. We propose the design of two such co-processors:
1) Data Structure Co-Processor (DSCP) to offload data structure computations to a separate core to increase sequential code performance; and
2) A Specialized Core to perform dynamic pointer bounds checking to support security.

Research Tool Development

Developed and maintain M-Sim 3.0 - a multi-core and multithreaded simulator of the Alpha ISA. The 3.0 version is a significant upgrade from prior versions. The code and supporting documentations are available at: www.cs.binghamton.edu/~msim
Presented a paper demonstrating the use of M-Sim in undergraduate architecture courses at the WCAE workshop in 2009.

Synergistic Activities

2007–Present Assistant Coach: ACM Student Chapter

- Trained students for ACM ICPC, TopCoder and local programming contests
- Promoted student participation in Topcoder, IEEExtreme and extracurricular programming
- In 2010, programming team placed in top third in Greater New York Region ACM Regional Collegiate Programming Contest (ACMGNYR)
- In 2009, programming team placed 3rd out of 53 teams in the ACMGNYR
- In 2008, programming team placed 1st out of 14 teams in the ACM Preliminary Programming Contest at Oswego, 4th out of 11 teams at the Northeast North America Programming Contest

2007–2010 Graduate Student Mentor for Research Experiences for Undergraduates: Lenny Domnister, Jack Choi, Jesse Elwell, Jared Schmitz. 2 papers published with these students.

2006–2007 Graduate Student Representative Search Committee for Dean of the Watson School

2008–2008 Graduate Student Representative for the Watson Student Advisory Committee

2008–2009 Graduate Student Organization: Computer Science Suborganization: Vice President

2009–2010 Graduate Student Organization: Computer Science Suborganization: 5th Officer

2010–2011 Graduate Student Organization: Computer Science Suborganization: Vice President

2009–2010 Graduate Student Representative: Undergraduate Task Force

April 16, 2011