1. Consider the following series of address references given as word addresses: 1,4,8,17,1,20,24,4,9,25,9,44,45. Assuming a direct-mapped cache with 16 one-word blocks that is initially empty, label each reference in the list as a hit or a miss and show the final contents of the cache. [15%]

2. Repeat problem 2 for a direct-mapped cache with four-word blocks and a total size of 16 words. [15%]

3. Repeat problem 2 for a two-way set-associative cache with one-word blocks and a total size of 16 words. Assume LRU replacement. [15%]

4. Repeat problem 2 for a fully associative cache with four-word blocks and a total size of 16 words. Assume LRU replacement. [15%]

5. Associativity usually improves the miss ratio, but not always. Give a short series of address references for which a two-way set-associative cache with LRU replacement would experience more misses than a direct-mapped cache of the same size. [20%]

6. Consider a virtual memory system with the following properties: 36-bit virtual byte address, 8KB pages, 32-bit physical byte address. What is the total size of the page table for each process on this machine, assuming that the valid, protection, dirty and use bits take a total of 4 bits and that all the virtual pages are in use? (Assume that disk addresses are not stored in the page table). [20%]